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**SPECIFICATIONS**

A multistage transistor amplifier was designed based on the specifications below:

* Power supply: ***+10V*** relative to the ground.
* Quiescent current drawn from the power supply: **no larger than 10 mA.**
* No-load voltage gain (at 1kHz): **|Avo|** = ***50 (± 10%)***
* Maximum no-load output voltage swing (at 1kHz): **no smaller than 8 V peak to peak**
* Loaded voltage gain (at 1 kHz and with RL = 1k):**no smaller than 90% of the no-load voltage gain**
* Maximum loaded output voltage swing (at 1kHz and with RL = 1k **no smaller than 4V peak to peak.**
* Input resistance (at 1 kHz): **no smaller than 20 k**
* *Amplifier type:* **inverting or non-inverting**
* Frequency response: **20 Hz to 50 kHz (-3dB response**)
* Type of transistors:**BJT**
* Number of transistors: **no more than 3**
* Resistances permitted: **values smaller than 220 from the E24 series*.***
* Capacitors permitted: **0.1 F, 1.0 2.2 4.7 , 10 , 47 , 100 , 220**
* Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE 404 lab kit.**

**NOTES**

* The output voltage must be free from distortions in all test conditions.
* The source resistance, Rs, must be 600 for all tests.

The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer’s choice. There are no restrictions in terms of using NPN or PNP transistors.

**PARAMETERS CONSIDERED**

* **VCC** = 10V
* **ITOTAL** <= 10mA
* **|Avo|** = 50 (± 10%) V/V
* **No load VO pk-pk** >=8V
* **|Av|** = 45 (± 4.5) V/V
* **Loaded VO pk-pk** >=4V
* **Rin** >= 20kΩ
* 20 Hz < **f** < 50 kHz
* **RS** = 600Ω
* **RL** = 1kΩ

**ASSUMPTIONS TAKEN**

* **BJTs** are in active mode.
* **2N3904** transistors are being used in the circuits.
* = 150
* **VBE\_ON** = 0.7 V
* **VCE\_SAT**= 0.3 V

Introduction

The three different BJTs are: common collector, common emitter, and the common base.

The common collector amplifier is usually used for voltage buffer, this amplifier has a voltage gain of unity. This is the reason why we use common collector as a voltage buffer. This amplifier has a configuration where the collector is common to the base and the emitter, like being common to the input and output circuit. So, this is cc configuration.

The common emitter amplifier usually has large inverse gain, which is small input and large output impedance. Common emitter configuration has an emitter in common with collector and base, like being common to the input and output circuit. So, this is ce configuration.

The common base amplifier has medium voltage gain which is large input and small output impedance. The current passing through the circuit uses the base as the common to the emitter and the collector, which make this a cb configuration.

Objective

The main goal of this project is to analyze the characteristics of the common emitter and common collector amplifier and learn the experimental procedures of the amplifier. This project is mainly based on the simulation of the amplifier.

Circuit under Test

In my design it is a CE-CC amplifier which is a common emitter followed by a common collector. CE amplifier which provides a large gain, and the CC amplifier buffers against the low load impedance of 1k to ensure a large enough overall gain and to maximize Vo pk-pk that meets with the specifications. CC amplifier also has a large input resistance unlike the CE amplifier which ensures a large overall input resistance since it depends on the input resistance of both amplifiers. The transistors used are **n-p-n.** *(2N3904)*

At the Common emitter amplifier, the resistors at the bases are very large to minimize the base currents and hence collector and emitter currents and to ensure a larger input resistance. The two resistances are equal to make calculations easier. The collector resistance was chosen to be 1kΩ to make VC large and the emitter resistance was chosen to be 220Ω to make VE small. VCE = VC – VE meaning that if VC is large and VE is small, it allows VCE to be large so that the BJT will be in active mode. At the emitter, an electrolytic 10 capacitor is placed in parallel with the emitter resistor along with two 10Ω resistors to minimize the resistance of the emitter during AC analysis which maximises the gain and input resistance. During DC analysis, capacitors are replaced with an open circuit flow through the 10 Ω resistors and only the emitter resistor is taken into consideration. At the Common collector amplifier, the resistors at the bases are also very large to minimize the base currents and hence collector and emitter currents and to ensure a larger input resistance. The two base resistors are equal to allow for easier calculations. There is no resistor at the collector to further minimize collector current and that will minimize the emitter current. A large emitter resistance of 22kΩ also minimizes the emitter current. In a CC amplifier, the output is taken from the emitter so a 100 electrolytic capacitor and the 1kΩ load are placed in parallel with the emitter resistor. DC analysis is made easier since no current will flow through the load. In AC analysis, the emitter resistor will be in parallel with the load.

To the left of the CE amplifier is a sinusoidal AC source with a source resistance of 600Ω and a 100 capacitor placed backwards. The frequency of the AC source is 1kHz. During DC analysis, the AC source is shut off and the capacitor also acts as an open circuit so that makes DC analysis easier. The capacitors are included in my design so that the waveforms of Vo and VI are smooth and they reduce clipping and noise in the waveforms. *The values chosen were based on trial and error in the simulation.* The capacitors also ensure that the frequency responses are within the range as noted at the specifications. All the resistors come from the E24 series.

Diagram

Description automatically generated

Circuit without the load

Graphical user interface

Description automatically generated

Oscilloscope result without the load

Diagram, schematic

Description automatically generated

Circuit with load

Graphical user interface

Description automatically generated

Oscilloscope result with the load

Experimental Result

Result from the common emitter circuit

|  |  |
| --- | --- |
| ***Simulation Values*** | ***Calculated Values*** |
| IB = 54.1 | IB = 47.5 |
| IC = 7.58 mA | IC = 6.83 mA |
| IE = 7.73 mA | IE = 7.16 mA |
| VB = 2.43V | VB = 2.31V |
| VC = 7.22V | VC = 7.93V |
| VE = 1.72V | VE = 1.67V |

In simulation BJT is active because Vce = 5.5V.

In calculation BJT is active because Vce = 6.26V.

Result from the common collector circuit

|  |  |
| --- | --- |
| ***Simulation Values*** | ***Calculated Values*** |
| **IB** = 2.28 | **IB** = 1.88 |
| **IC**= 288 | **IC**= 287 |
| **IE** = 297 | **IE** = 2.96 |
| **VB** = 7.23V | **VB** = 7.3V |
| **VC** = 10V | **VC** = 10V |
| **VE** = 6.51V | **VE** = 6.48V |

Total

|  |  |
| --- | --- |
| ***Simulation Values*** | ***Calculated Values*** |
| **|Avo| =** 47.43 | **|Avo| =** 50 |
| **|Av| =** 46.89 | **|Av| =** 46.234 |
| **Itot =** 8.23mA | **Itot =** 7.56mA |

Conclusion Remark

The simulation value will always differ from the calculated values because of human errors. We can see noticeable difference in common emitter amplifier and the other values. For the common collector amplifier, the calculated values and the simulation values are almost equal. The total current exceeds 10mA in the calculation part and there are some errors caused by current in simulation, this is because capacitors have internal resistance, and the resistors are not ideal resistors. In calculations the capacitors are shorted for AC analysis also the temperature also effects on how the transistor works. The assumed values could also affect the result obtained from the transistor.